AMENDMENTS TO THE SPECIFICATION

Please amend paragraphs 0031-0034, 0036, 0038, and 0040 as follows:

[0031] Reference is now made to Fig. 2 of the drawings, a block diagram of the circuitry on ~~chips 14 and 16~~Chip 1 (14) and Chip 2 (16), as well as clock routes 34 and 36, for maintaining a synchronized relationship between the clock waves of ~~chips 14 and 16~~Chip 1 (14) and Chip 2 (16), at terminals 22 and 24, so that the clock waves at these terminals have a synchronized phase relationship.

[0032] The clock circuitry in proximity to the left edge 23 of [[c]]Chip 1(14), where the clock wave from clock source 12 is introduced or derived, includes voltage controlled delay circuit [[25]]84. Circuit [[25]]84 has a clock input terminal connected to be responsive to the clock source and a clock output terminal that supplies the clock wave delayed by circuit [[25]]84 to a clock input of buffer and gater [[27]]70, constructed as described in the previously mentioned patent. The clock circuitry in proximity to edge 23 also includes phase detector and low pass filter circuit [[29]]80, and voltage controlled delay circuit [[31]]74, as well as buffer and gater [[33]]82. Buffer [[27]]70 has a clock output terminal connected to supply a clock wave to a clock input terminal of circuit [[31]]74, having a clock output terminal connected to drive a clock input terminal of buffer [[33]]82. Phase detector [[29]]80 has first and second clock input terminals, respectively connected to be responsive to the clock waves of clock source 12 and at the output

terminal of buffer and gater [[33]]82. Detector [[29]]80 responds to the clock waves at the first and second clock input terminals thereof to derive a DC signal voltage having an amplitude and polarity respectively indicative of the magnitude and direction of the relative phase angles of the clock waves derived from clock source 12 and buffer [[33]]82. Detector [[29]]80 supplies the DC signal voltage it derives to control input terminals of delay circuits [[25]]84 and [[31]]74 to increase and decrease the delay times of circuits [[25]]84 and [[31]]74, relative to nominal delay values thereof. The output of detector [[29]]80 thus maintains the phases of the clock outputs of clock source 12 and buffer [[33]]82 synchronized at a predetermined phase angle 90°, 180°, 270° or 360°, to maintain phase synchronization for the clock outputs of circuitry ~~25, 27, 31 and 33~~84, 70, 74, and 82.

[0033] Typically [[c]]Chip 1 (14) includes several cascaded subsequent sections with clock circuitry the same as described in connection with circuit elements ~~25, 27, 29, 31 and 33~~84, 70, 80, 74, and 82. In such cases, the clock output of buffer [[27]]70 functions the same as the clock wave of clock source 12 to drive clock inputs of the subsequent sections. Thus, the output of buffer [[24]]70 drives (1) a delay circuit corresponding to delay circuit [[25]]84 and (2) a phase detector and low pass filter corresponding to phase detector and low pass filter [[29]]80. For convenience these subsequent sections are not illustrated, except for the last section. In the subsequent discussion, the output of circuit [[27]]70 is assumed to be connected to the last section of [[c]]Chip 1 (14) in the same way the ~~output~~clock source 12 is connected to the first section.

[0034] The clock circuitry of the last section of [[c]]Chip 1 (14) includes, in proximity to terminals 22 and 24 and edge 26, buffer and gater circuit 70. Circuit 70 includes logic circuitry for selectively coupling clock waves to circuitry on [[c]]Chip 1 (14) in proximity to buffer and gater 70. In addition, buffer and gater circuit 70 includes output terminal 72 which is in proximity to and connected to terminal 22, which is essentially on edge 26. Buffer and gater 70 has a clock input terminal 71 connected to be responsive to a clock wave at output terminal 73 of voltage controlled delay circuit 75, located in proximity to buffer and gater 70. Circuit 75 has a clock input terminal 77 responsive to a clock wave derived on a portion of [[c]]Chip 1 (14) upstream of and in proximity to circuit 75 and ultimately in response to the clock wave from clock source 12. In the illustrated circuit of [[c]]Chip 1 (14), the output of buffer and gater 27 is connected to clock input terminal 77 of voltage controlled delay circuit 75.

[0036] To maintain synchronism between the clock waves at terminals 22 and 24, [[c]]Chip 1 (14) includes phase detector and low pass filter 80, having a first clock input terminal ~~81~~ responsive to a clock wave that ultimately is derived on chip 14 in response to an output of source 12. In the illustrated circuit, terminal 81 is connected to the clock output of buffer and gater 27. Chip 14 includes the previously described circuitry for maintaining synchronization between the output of clock source 12 and the clock input of detector and filter 80 at the first clock input terminal ~~81~~. Detector and filter 80 has a second clock input terminal 83 responsive to the clock wave at the output terminal of buffer and gater 82, having an input terminal connected to

be responsive to the clock wave that voltage controlled delay circuit 74 supplies to terminal 78.

[0038] The clock wave that buffer and gater 70 supplies to terminal 22 propagates to terminal 28 of [[c]]Chip 2 (16) via clock route 34. The clock wave that route 34 applies to terminal 28 drives clock circuitry in a first stage of [[c]]Chip 2 (16) that is similar to the first stage of [[c]]Chip 1 (14). In particular, a first stage of [[c]]Chip 2 (16) includes phase detector and lowpass filter 88, buffer and gater circuit 90, voltage controlled delay circuits 92 and 94 as buffer and gater 96, that respectively correspond to detector [[29]]80, buffer and gater [[33]]82, delay circuits [[31]]74 and [[25]]84 and buffer and gater [[22]]70. Hence, [[c]]Chip 2 (16) responds to the clock wave at terminal 28 in the same way that [[c]]Chip 1 (14) responds to the clock wave from clock source 12 and the clock output of route 34 is the clock input of [[c]]Chip 2 (16).

[0040] Chip 2 (16) can, but does not necessarily, include several additional cascaded stages, one of which is illustrated as being the same as (1) the last stage of [[c]]Chip 1 (14) and (2) the same as the first stage of [[c]]Chip 2 (16), except that the last stage of [[c]]Chip 2 (16) includes buffer and gater 98 that drives clock route 40 via terminal 46 and voltage controlled delay 99 that responds via terminal 44 to the output of clock 38. It is to be understood that if [[c]]Chip 2 (16) is so small that it includes only a single stage so buffer and gater 98 and delay circuit 99, as well as the other circuits of the illustrated last stage are omitted, the output of buffer and gater 96 is connected directly to terminal 42 and the input of delay circuit 92 is connected directly to terminal 44.